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10/743,104	12/23/2003	Mitsuhiko Ogihara	MAE 305	8001

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
3663	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,104	OGIHARA ET AL.	
	Examiner	Art Unit	
	JOHANNES P. MONDT	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5,6,9,10,18,20,37 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6,9,10,18,20,37 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *April 2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/9/08 has been entered.

Response to Amendment

2. Amendment filed 7/9/08 together with said Request for Continued Examination forms the basis for this Office Action. In said Amendment Applicants substantially amended the Specification, canceled claims 2 and 38, substantially amended claims 5, 6 and 37 and thereby claims 5, 9, 10, 18 and 20 dependent thereon, and added new claim 39.

Comments on "REMARKS" filed with said Amendment are included below under "Response to Arguments".

Specification

The following is a quotation of 35 U.S.C. 132 (a):

> Whenever, on examination, any claim for a patent is rejected, or any objection or requirement made, the Director shall notify the applicant thereof, stating the reasons for such rejection, or objection or requirement, together with such information and references as may be useful in judging of the propriety of continuing the prosecution of his application; and if after receiving such notice, the applicant persists in his claim for a patent, with or without amendment, the application shall be reexamined. No amendment shall introduce new matter into the disclosure of the invention.

3. The Amendment to the Specification is objected to for the introduction of new matter: the limitation *"inorganic compound"*, newly introduced by amendment on page 11, line 7, constitutes new matter, because although the examples of "other materials" as previously disclosed are inorganic semiconductor materials, these materials have not been disclosed to be compounds, and in fact they are not (see, e.g., "The Columbia Encyclopedia", Columbia University Press 2004 for the definition of "chemical compound"). Furthermore, it is noted that although original claim 16 now canceled recited said semiconductor thin film to be a compound semiconductor material, it did not claim said semiconductor thin film to be an *inorganic* compound. Applicant is required to cancel the new matter in any responsive reply to this Office Action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly introduced limitation "said semiconductor thin film being made of an inorganic compound semiconductor as a main material" (lines 15-17 of claim 5) does not find support in the

specification as originally filed. The reasons for this rejection are the same as the reasons for the objection to the Specification under 35 USC 132(a) (see section 3 above).

6. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly introduced limitation that "said semiconductor thin film being disposed so as not to extend outward from edges of the metal layer" (claim 5, lines 17-18) does not find support in the specification as originally filed.

7.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The lack of support noted above in section 5 above for the newly introduced limitation "said semiconductor thin film being made of an inorganic compound semiconductor as a main material" (lines 15-17 of claim 5) in the specification renders the metes and bounds of said limitation vague and ill-defined, causing the claims to be indefinite.

10. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The lack of support noted above in section 6 above for the newly introduced limitation "said semiconductor thin film being disposed so as not to extend outward from edges of the metal layer" (lines 17-18 of claim 5) in the specification renders the metes and bounds of said limitation vague and ill-defined, causing the claims to be indefinite.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. ***Claims 5 and 37*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al (6,242,324 B1).

Kub et al teach a combined semiconductor apparatus (see title and first sentence of abstract; see Figures 3 and 5, col. 9, l. 36 – col. 11, l. 18), comprising: a silicon substrate 12 having a CMOS integrated circuit formed therein ("CMOS" = complementary metal on silicon) (col. 9, l. 36), the silicon substrate having a rough or irregular surface due to at least a wiring pattern of the integrated circuit (the wiring is the interconnect structure 36 or 68: see col. 9, l. 2-13 , col. 11, l. 16+, and Figures 3 and 5);

a planarized region 22 (col. 9, l. 36-38; Figure 3) defined over said rough or irregular surface of said silicon substrate in Figure 3, while although oxide region 56 in Figure 5 is not expressly referred to as planarized, it would at least have been obvious to try since layer 56 is introduced in Kub et al as "the" oxide layer 56, antecedent basis only being available through the previous embodiments, which all feature a planarized oxide layer (such as 22 in Figure 3) at the same relative position to other layers, while the same technology (CVD followed by CMP (col. 9, l. 3-5) as employed for layer 22 can be applied with reasonable expectation of success, which renders "planarized" for region 56 in Figure 5 obvious (see MPEP 2141) (N.B.: the embodiment of Figure 5 is characterized as "similar" to that of Figure 2 (col. 10, l. 49-52) wherein the layer similar to 56, i.e., layer 22 is planarized (col. 9, l. 3-5));

a substantially planar metal layer 38 or 54 (col. 9, l. 38-39, col. 10, l. 66- col. 11, l. 9) disposed over said planarized region (Figures 3 and 5); and

a semiconductor thin film 40 or 50/58 (col. 9, l. 63+, col. 10, l. 66+), or, in alternative interpretation 40/44/46 or 50/58/64/66 (N.B.: CdTe is an inorganic compound semiconductor) disposed over said metal layer and including an optoelectronic element

(CdTe/HgCdTe material layers 44/46 are comprised in a photo-detector in Figure 3, or similar material layers 64/66 of photo-detectors in Figure 5: see col. 9, l. 65+ and col. 11, l. 13+, resp.) and being wafer bonded (col. 9, l. 64) on grown on top of said metal layer (through layer 42 in the case of layer 40) and disposed over the integrated circuit (Figures 3 and 5) and said metal layer electrically connects said optoelectronic element to said integrated circuit (col. 9, l. 38 - col. 10, l. 13).

Furthermore, although the illustrated and detailed embodiments by Kub et al are drawn to the photo-detector art, Kub et al expressly state that "other semiconductor thin film crystal layers" such as "GaAs" and "InP" can be bonded to the metal layer for making a light-emitting diode (LED) (see col. 10, l. 29-46) (GaAs and InP are both inorganic compounds). The limitation "light-emitting element" is thus obvious over Kub et al itself, in particular their suggestion to use the approach described in the detailed description also to the art of LEDs. *Motivation* for including said suggestion derives from the profit advantage of maximizing the range of applicability of the invention along the suggestion of its inventors.

Finally, the limitation that said semiconductor thin film "not extending outward" as recited in the final lines is met when formed by wafer bonding on said metal layer, because any portion sticking out is by necessity not bonded to the wafer. The process of wafer bonding is furthermore obvious also for the embodiment of Figure 5 as alternative, at least as a method obvious to try (MPEP 2141), because the type of material involved are the same.

On claim 37: additionally, Kub et al teach with respect to the embodiment of Figure 3 that a thin oxide layer 42 may be used (optionally) to cover the metal layer (col. 9, l. 42-62), but that in any case it is "likely necessary" that the surface of the resulting structure be CMP polished to small surface roughness (which implies "planarized") (loc.cit.). In the presence of 42 this implies that the metal layer and the inter-dielectric layer 42 form a planarized film. With regard to the limitation "the same thickness" applicant is further reminded that it has been held that Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

14. ***Claims 9, 10 and 18*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al as applied to claim 5 above, and further in view of either Walsh (US 6,351,327 B1) or Tohyama et al (US 6,433,367 B1). As detailed above, claim 5 is unpatentable over Kub et al. Kub et al do not necessarily teach the further limitation as defined by claim 9; however it would have been obvious to include said further limitation in view of Walsh, who, in art on the application of CMOS technology to integrated LED driver and LEDs (67 and 69-71, resp.) (col. 3, l. 9-24), teach the application of a common electrode layer 33 (col. 4, l. 6-15) on a surface of a semiconductor thin film 39 (loc.cit.) opposite to the surface on which the light-emitting element (69-71) is formed. See Figures 1 and 2). The application of the teaching of a common electrode when

included in the invention by Kub et al meets the claim limitations and would have been obvious as only one common reference voltage is needed to drive the LEDs. *Motivation* stems from economy of construction.

Similarly, Tohyama et al disclose an LEDs 13 with common electrode 17 (Figure 1 and col. 2, l. 55 - col. 3, l. 34) in integrated circuitry on the second surface 10e of the LED chip array. The application of the teaching of a common electrode when included in the invention by Kub et al meets the claim limitations and would have been obvious as only one common reference voltage is needed to drive the LEDs. *Motivation* stems from economy of construction.

On claim 10: said integrated circuit includes individual electrode terminals 36 or 68 (see Figures 3 and 5; col. 9, l. 12-14 and col. 11, l. 10-18 in Kub et al); and said apparatus comprises individual interconnecting lines formed on a region extending from an upper surface of said light-emitting element to said individual electrode terminals (see top portion of Figures 3 and 5; loc.cit. in Kub et al).

On claim 18: in the combined invention as defined above, said light-emitting element is a plurality of light-emitting elements arranged in said semiconductor thin film.

15. ***Claim 20*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al as applied to claim 5 above, and further in view of Tohyama et al (US 6,433,367 B1).

Although Kub et al do not necessarily teach the further limitation defined by claim 20, the application of optical printer head would have been obvious over Tohyama et al, who, in a patent on an LED array chip (title, abstract and col. 2, l. 55 – col. 3, l. 34), hence art analogous to Kub et al, teach the application to an optical printer head (col. 3,

l. 23-34 and their claim 11). *Motivation* to include the teaching by Tohyama et al in this regard is the obvious advantage to apply a device to a function when it is demonstrably capable of performing the function.

16. ***Claims 39 and 6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al as applied to claim 5 above, and further in view of Ferra et al (US 2002/0155795 A1). As detailed above, claim 5 is unpatentable over Kub et al. Kub et al do not teach the further limitations by claim 39 and 6. However, it would have been obvious to include said limitations in view of Ferra et al, who, in a patent application drawn to the use of a CMP tool for planarizing layers (title, abstract), hence analogous to the planarization aspects in Kug et al, teach (1) the inclusion of a metal barrier layer between metal lines 101 on the one hand and an underlying wafer 100 and neighboring dielectric 103 on the other hand, so as to prevent the metal in the metal layer from migrating into a neighboring dielectric (see [0036]), and (2) the planarization of both barrier layer and metal layer ([0036]-[0039]). Hence said barrier layer 102 meets the limitation planarized film, while, when implemented in the invention by Kug et al said planarized film is disposed on a planarized region, wherein said metal layer is disposed on said planarized film. With regard to claim 6, said planarized film 102 is an interdielectric film. Motivation to include the barrier film in Kug et al derives from the resulting advantage of the prevention of migration of metal into the dielectric planarized region (CVD oxide 22 in Kug et al) as taught by Ferra et al. The inclusion of the teaching on planarizing both barrier and metal layers would at least have been obvious because the technique for improving a particular class of devices was part of the

ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

Response to Arguments

17. Applicant's arguments filed 7/9/08 have been fully considered but they are not persuasive.

Issues of 35 USC 112 and Specification: Although a previous rejection under 35 USC 112 was overcome by amendment, said amendment introduced several issues of new matter, with reference to the rejections under 35 USC 112, first paragraph, overhead. In compliance with the directive to nevertheless search the newly claimed invention, rejections are being provided for the newly amended claims. The citation of new art in this regard in no way implies admission of any lack of validity of the previous rejections over the previous claim language. Applicant's argument that the amendment introducing the term "inorganic compound semiconductor" is supported by the original specification (page 8 of Remarks) is not persuasive, because none of the materials cited in the argument are necessarily compounds, for which a definite ratio ordained by the valences of the atomic constituents would have to determine a fixed stoichiometric ratio. See, e.g., "The Columbia Encyclopedia", Columbia University Press 2004 for definition of "chemical compound". Applicant additional argument that the amendment were further supported by the specification reciting "the semiconductor substrate may be made of other materials such as amorphous silicon, single crystal silicon, polysilicon, compound semiconductor or organic semiconductor" delineates a set of materials that does not specifically include all inorganic compound semiconductors. For the same

reason the amendment to the Specification is objected to for introducing new matter. Furthermore, applicant refers to Figures 13-16 and 19-22 only for the support of the limitation on the semiconductor thin film not extending outward. However, said Figures only "a part" or a "cross-section", or they show an intermediate rather than final structure, or they show only a schematic view. The Figures as a whole do not provide any evidence or disclosure that the newly introduced limitation on the semiconductor thin film not extending outward was met in the invention as originally filed.

Issues of 35 USC 103(a): All arguments by applicant pertain to the previous rejections based on the previous claim language. In compliance with the newly presented claim language, new art had to be cited. Arguments with regard to the rejections over Konuma are thus moot; however, in no way does this mean any admission on persuasiveness of any traverse if applied to the previous claim language.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/
Primary Examiner, Art Unit 3663